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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,511	03/10/2000	Yasushi Kubota	49639(820)	4950

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EXAMINER	
DINH, DUC Q	

ART UNIT	PAPER NUMBER
2674	20

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/523,511	Applicant(s) KUBOTA ET AL.	
	Examiner DUC Q DINH	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6,11,13,15,17,19,21,23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-3, 6, 11, 13, 15, 17, 19, 21, 23, and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Amendment Filed on May 25, 2004, an Office Action is provided as following.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. (U. P. Patent No. 6,266,041), hereinafter, Cairns

In reference to claim 2, Cairns discloses in Fig. 3 a shift register comprising: a plurality of DFFs circuit 21 (corresponding to the claimed latch circuits), clock signal line CK transmitting a clock signal, a plurality of switching circuits for performing electrical connection and disconnection between the clock signal line CK and at least one of the plurality of DFFs circuits according to the control signals (start signals) provided at the left most (at power on) of the DFFs circuit and a other signals separated from the start signal for provided from the output of the left most DFF circuit (corresponding to the cyclic signals provided at regular interval) and the output of the output of the second DFF circuit and so on.

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to recognize that the left most switching circuit 23 electrically disconnects the left most the plurality of DFFs circuits from the clock signal at power on and the output of DFFs circuits as the cyclic signals at regular intervals determined by the output of the OR gates as

shown in Fig. 3 for enabling the clocking rate of the shift register to be reduced and also to minimize the capacitive loading of the clock lines or lines and the power consumption of the circuit, it is known to apply state-controlled clock schemes to the shift register (col. 2, lines 20-32). Moreover, FIG. 3 shows a data line driver circuit 20 in which the input and output of each DFF 21 is coupled to a respective input of an associated OR gate 22 which controls a pass gate 23 so as to ensure that only the required DFF's 21 are clocked by each clock pulse (col. 2, lines 41 – 46).

4. Claim 3, 6, 11, 13, 15, 17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns as applied to claim 2 above, and further in view of Ogawa (U. P. Patent No. 6,018,331).

In reference to claim 3, Cairns discloses the signals HSYNC is vary in accordance with the pulse signal transferred and a plurality of switching circuit 23 each connect and disconnect corresponding to the latch circuit to/from the clock signal line CL. However, Cairns fails to discloses in at least one part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has frequency lower than a normal operation mode. Ogawa discloses in FIG. 5A, which shows a block diagram of source driver 104, start pulse (DX) 202 is supplied to the shift input of shift register 204. This start pulse (DX) 202 is sequentially shifted within shift register 204 in accordance with shift clock (CLX) 201. This shift output is supplied to each individual AND gate 207 opened by enable signal 203. The output of each AND gate 207 is supplied to the source line 206 of each picture element 205.

In addition, as discloses Fig. 8, in one part of the least one part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has frequency lower than a normal operation .

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to applied the method of frame display control of Ogawa in the device discloses by Cairns for providing an image display device that when displaying image signals having a number of picture elements fewer than the number of picture elements in the image display device in the center of the display device, and displaying a frame around the periphery of the displayed image, can display the frame adequately even in cases in which the input signals have a short horizontal blanking interval (col. 3, lines 10-15).

In reference to claim 6, Ogawa discloses the frequency difference as claimed

In reference to claims 11, Cairns discloses that as the shift register 51 is clocked by the clock signal CK, the state of each DFF 52 is passed to the next DFF along the register 51, and the effect of such clocking on the output C of the third DFF 52 from the left in the detail B is shown in the timing diagram of FIG. 7b, together with the clock signal CK and the horizontal synchronization signal HSYNC. It will be appreciated that the output C incorporates a series of pulses of the duration of one period of the clock signal CK corresponding to each `1` level separated by gaps of three clock periods corresponding to the three consecutive `0` levels, as well as a pulse of two clock periods corresponding to the two consecutive `1` levels. The form of such an output C is particularly useful for controlling each line driver 54 as will be described in more detail below. Since such a circuit will tend to cause adjacent line drivers 54 to commence their operative cycle at data rate clock intervals, this will have the effect of smoothing the power

dissipation of the circuit. As a result the circuit may bring about a reduction in the amount of voltage supply compensation and minimize switching interference on the data lines (col. 7, line 59 – col. 8, line 3).

In reference to claim 13, Cairns discloses in FIG. 4 shows the general architecture of a digital line-at-a-time data line driver circuit 30 which comprises an input register 31 to which digital video data is supplied in 6 or 8 bit RGB format, a storage register 32 in the form of digital latches, and digital-to-analogue converters 33 connected to the outputs of the storage register 32 and supplied with reference voltages for applying data to the data lines by way of output buffers 34. As the digital data bits are supplied to the input register 31, they are stored in the register 32 and, when a whole line of data has been stored, the contents of the input register 31 is transferred to the storage register 32 in order to control the D/A converters 33. In the case of small screen displays, the D/A converters may be connected directly to the data lines so as to charge the data lines by simple charge sharing, although output buffers are required for higher performance displays. Control logic 35 is provided for controlling the input register 31, the storage register 32, the D/A converters 33 and the buffers 34 on receipt of appropriate control signals (col. 3, lines 4-21).

In reference to claim 15, Cairns discloses that the drive circuit comprising clock means for generating a clock signal, a shift register comprising a chain of control shift elements having respective outputs, and a series of driver stages coupled to said outputs and controllable by control signals for sampling an input signal and for supplying the sampled signals to a corresponding series of lines, wherein each of the driver stages is associated with a respective one of the control shift elements and is locally controlled by a plurality of different control

signals derived from signals generated by said one control shift element and/or at least one local control shift element in the vicinity of said one control shift element in the shift register in response to clocking of the shift register by the clock signal (col. 4, lines 12-26).

In reference to claims 17, 19, 21, Ogawa discloses an LCD having data driver and scan driver comprising a shift register circuit as claimed.

5. Claims 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns and Ogawa as applied to above claims, and further in view of Ino et al. (U. P. Patent No. 5,903,014), hereinafter Ino.

In reference to claims 23 and 25, Cairns and Ogawa fail to disclose the process to form the data driver. Ino discloses that semiconductor devices each having integrated thin film transistors and the like are particularly suitable for driving substrates of active matrix type electro-optical devices, and therefore, they are being extensively developed at present. A thin film transistor has a semiconducting thin film as an active layer, which is made from amorphous silicon or polycrystalline silicon. The polycrystalline silicon transistor is superior in electric characteristics such as a carrier mobility to the amorphous silicon transistor, and it can be used for a peripheral driving circuit as well as for a switching element. In this regard, studies are being actively conducted on the polycrystalline transistors. On the other hand, when used for an active matrix display which is one example of the active matrix type electro-optical devices, the semiconductor device must adopt an inexpensive large-sized insulating substrate. From this viewpoint, there is a strong demand to develop a low temperature process capable of forming thin film transistors at a temperature in a range of 600.degree. C. or less, preferably, 400.degree.

C. or less. Laser annealing or ion doping becomes important for the low temperature process. Moreover, from the standpoint of the structure, the thin film transistor is classified into a bottom-gate type (reversely staggered type) and a top-gate type. The bottom-gate type is superior to the top-gate type in terms of compatibility with the low temperature process (col. 1, lines 19-40).

It would have been obvious to use the process to produce the thin film transistor disclosed by Ino to make the data driver in the device of Cairns and Ogawa because it would provide the polycrystalline silicon transistor is superior in electric characteristics such as a carrier mobility to the amorphous silicon transistor, and it can be used for a peripheral driving circuit as well as for a switching element (col. 1, lines 19-25).

Response to Arguments

6. Applicant's arguments, see pages15-22, filed on 5/25/04 have been fully considered. With respect to the 112 First Paragraph have been fully considered and are persuasive. The Rejection of claims 2-3, 6, 11, 13, 15, 17, 19, 21, 23, and 25 has been withdrawn. With respect to the 103(a) Rejection as applied to claims 2-3, 6, 11, 13, 15, 17, 19, 21, 23 and 25 Cairns as discloses in Fig. 3 a plurality of switching circuits for performing electrical connection and disconnection between the clock signal line CK and at least one of the plurality of DFFs circuits according to the control signals provided at the left most of the DFFs circuits and a other signals separated from the start signals for provided from the output of the left most DFF circuit (corresponding to the cyclic signals) and the output of the output of the second DFF circuit and so on (cyclically provided to the OR circuit to disconnect one after the other DFF circuits). It would have been obvious for one of ordinary skill in the art at the time of the invention was made to recognize that the left most switching circuit 23 electrically disconnects the left most the

plurality of DFFs circuits from the clock signal at power on and the output of DFFs circuits as the cyclic signals at regular intervals determined by the output of the OR gates as shown in Fig. 3 for enabling the clocking rate of the shift register to be reduced and also to minimize the capacitive loading of the clock lines or lines and the power consumption of the circuit, it is known to apply state-controlled clock schemes to the shift register as suggested in col.2, lines 20-32 of Cairns. Therefore, the rejection is maintained.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Allowable Subject Matter

8. Claims 1, 5, 8-10,12, 14, 16, 18, 20, 22, 24 and 35-45 are allowed (as indicated in the previous Office Action).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **DUC Q DINH** whose telephone number is **(703) 306-5412** The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD A HJERPE** can be reached on **(703) 305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivery response should be brought to: Crystal Park II, 2121 Crystal Drive, Arlington, Va Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

DUC Q DINH
Examiner
Art Unit 2674

REGINA LIANG
PRIMARY EXAMINER

DQD
August 17, 2004